Next Generation Quantum Annealing System

Qubits North America
Newport, RI

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D-Wave Systems Inc.

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D:Wave
The Quantum Computing Company™

The Next Generation quantum annealing system will have

- A more powerful processor
  - 5000 qubits - to solve larger problems
  - Increased connectivity - to make easier posing of complex problems
  - Lower noise technology
    - *more accurate problem specification*
    - *higher performance annealing*
- Improved operating software
- A hybrid developer environment

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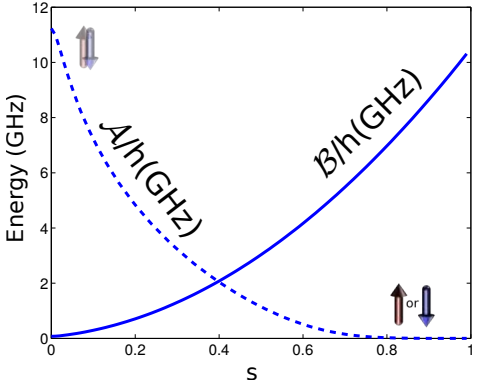
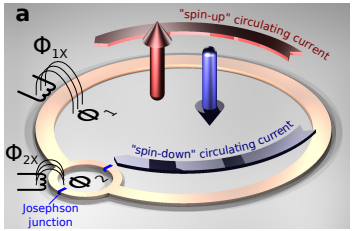
Quantum mechanics helps find the optimum

The goal of quantum annealing (QA): model the Hamiltonian

$$\mathcal{H}_S(s) = -\frac{\mathcal{A}(s)}{2}\sum_i \sigma_{x,i} + \frac{\mathcal{B}(s)}{2}\left[-\sum_i h_i\sigma_{z,i} + \sum_{i<j} J_{ij}\sigma_{z,i}\sigma_{z,j}\right]$$





- T. Kadowaki and H. Nishimori, PRE, **58**(5), pp. 5355-5363, (1998)
- E. Farhi, *et al.*, Science **292**, 472 (2001)
- W. Kaminsky, S. Lloyd, T. Orlando, **arXiv:quant-ph/0403090**, "Scalable Superconducting Architecture for Adiabatic Quantum Computation"

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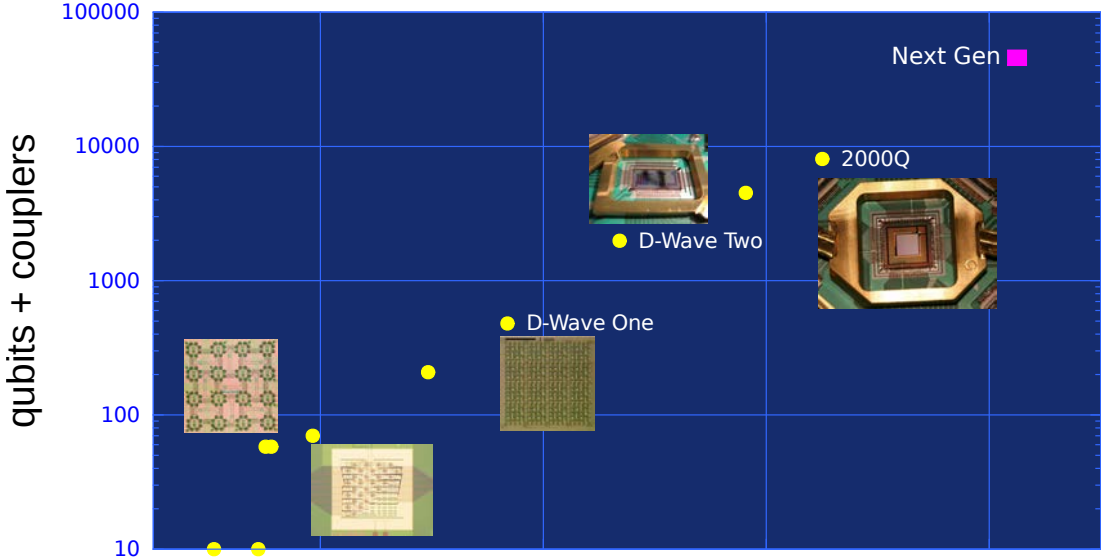
Progression of processor scale over time



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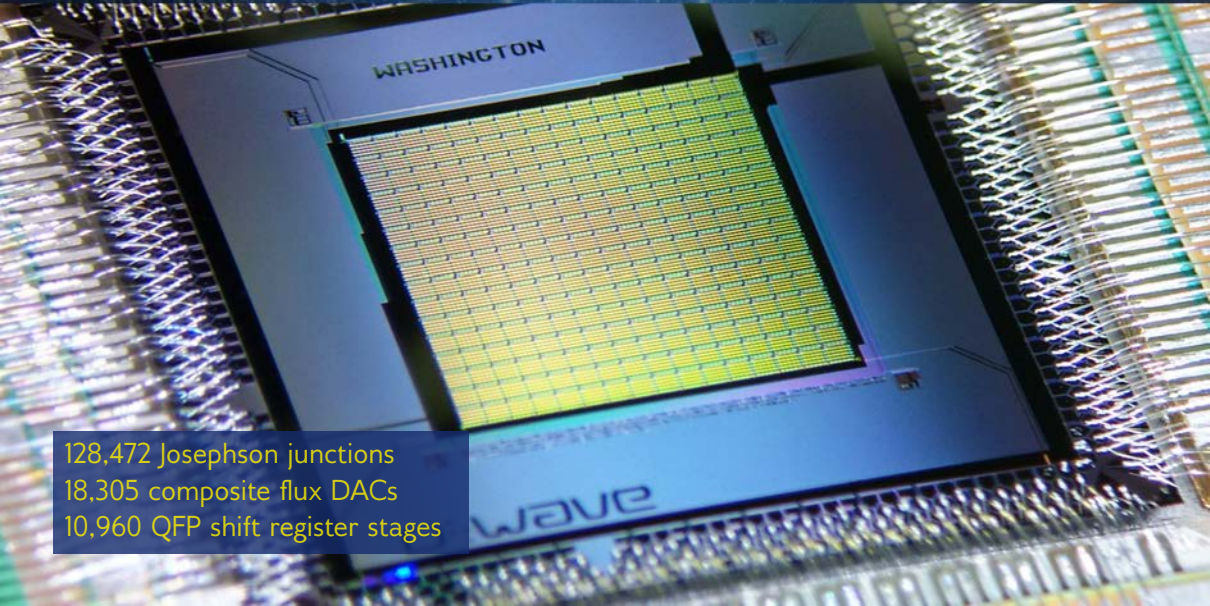
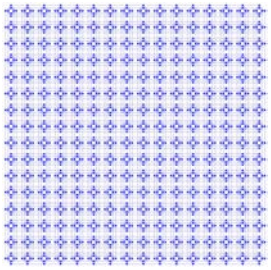
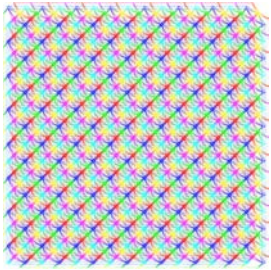
D-Wave 2000Q quantum annealing processor



128,472 Josephson junctions
18,305 composite flux DACs
10,960 QFP shift register stages

Advantage™ qubits are more connected

2000Q		Advantage
		
2000	Qubits	5000
6000	Couplers	40000
128,000	Josephson Junctions	1,030,00
42 m	Wiring	110 m
$(5.5\ \mathrm{mm})^2$	Active Area	$(8.4\ \mathrm{mm})^2$
22 kiloByte	On-chip memory	130 kiloByte

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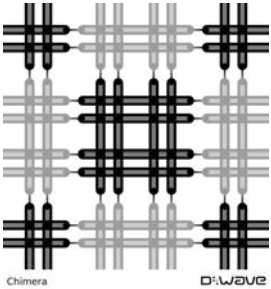
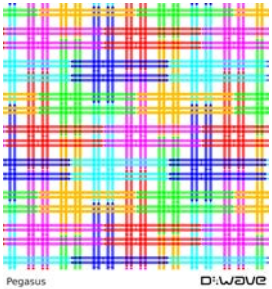
A closer look ...

2000Q



Advantage



6 Connections/Qubit **15**

The new graph, and embeddings on it can be explored now in the Ocean tools: `ocean.dwavesys.com`

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Basic graph embedding statistics

	2000Q	Advantage
Complete Graph	64 (17)	180 (17)
Complete Bipartite	64x64 (16)	172x172 (15)
Cubic Lattice	8x8x8 (4)	15x15x12 (2)
Factoring Circuit	16-bit (16)	30-bit (15)

(max chain length)

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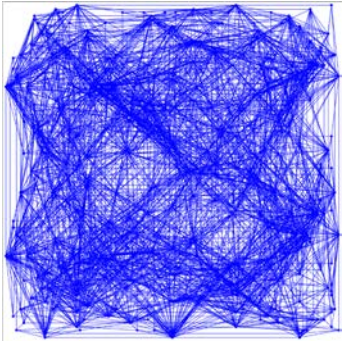
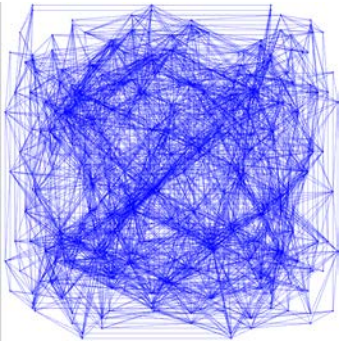
Compare embedding of graphs with similar average degree

Chimera C16 - DW 2000Q



Pegasus P6 - 680 Qubit Prototype



Logical Qubits	366	318
Average chain length	5.6	2.1
Average degree	24	25

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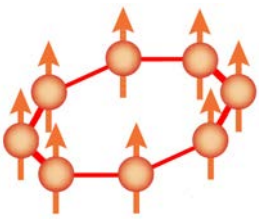
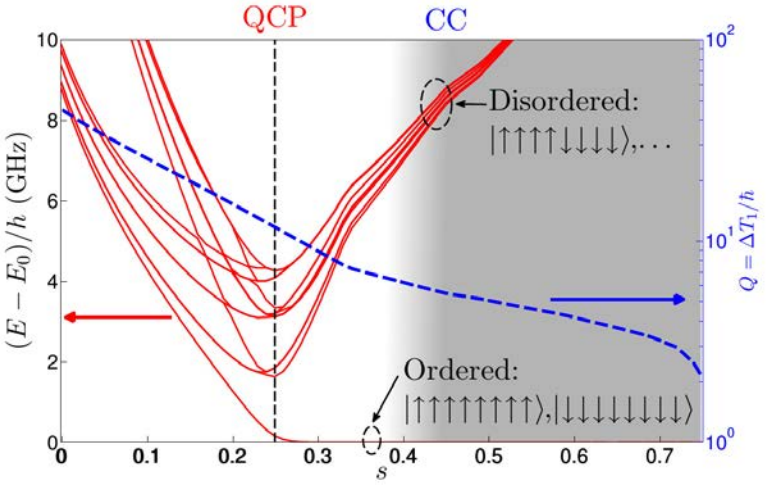
Why do we want to reduce device noise?

- Better control of problem and anneal specification
- Better performance of QA



"Quality" factor

$$Q = \mathcal{A}(s) T_1(s)/\hbar$$



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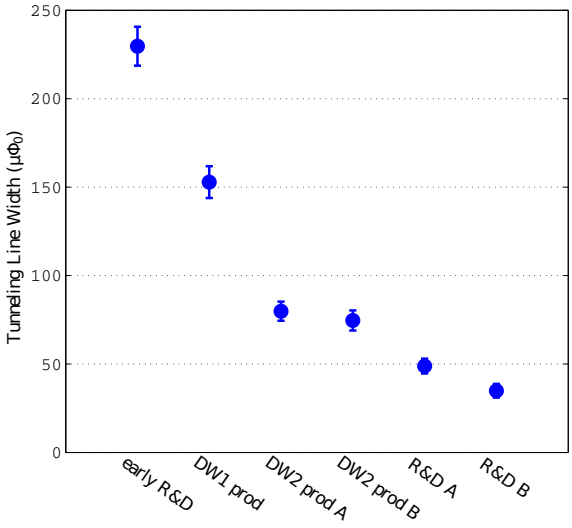
In pursuit of a lower noise technology

Regularly measure:

- low frequency flux noise
- 0th order Macroscopic Resonant Tunnelling (MRT) peak:
  (a measure of integrated high frequency $S_\Phi(\omega)$)

Ongoing program to reduce intrinsic noise:

- Test ~ 250 samples per year
- monitor process stability
- modify processes and materials



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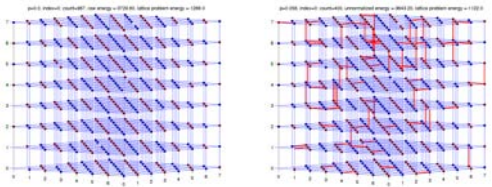
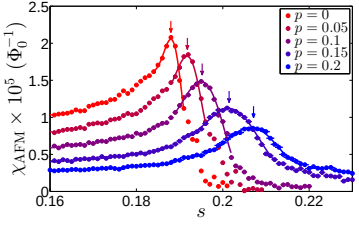
Quantum simulation

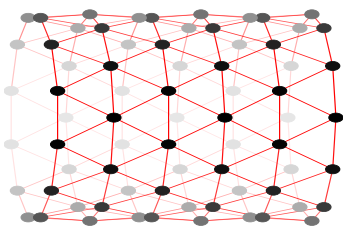


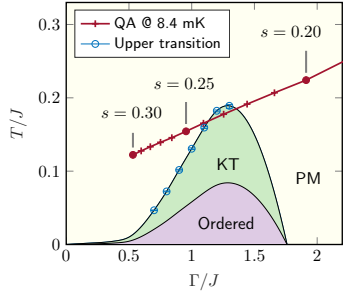
$$\mathcal{H}_{3D}(s) = -\frac{\Gamma(s)}{2}\sum_i \sigma_i^x + \mathcal{J}(s)\sum_{\langle i,j\rangle} J_{ij}\sigma_i^z\sigma_j^z$$



transverse field cubic Ising lattice

topological phase transition





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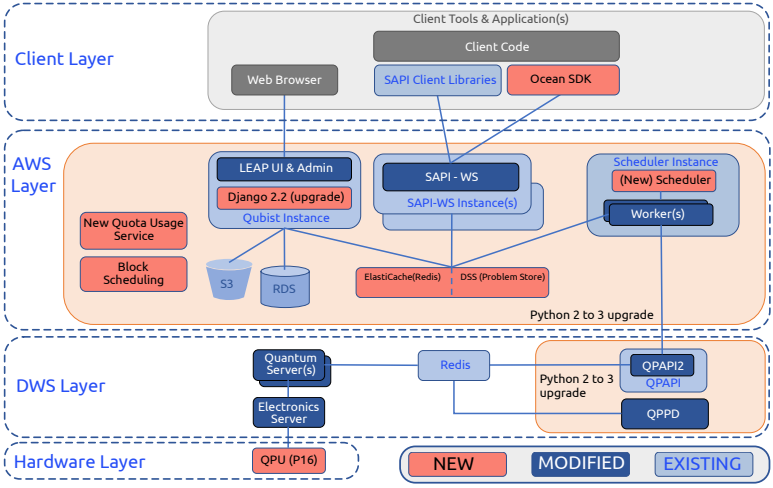
New operating software to provide better support for hybrid applications



- architecture
- latency
- scheduling

We believe the first quantum application that will bring value to a customer will use a hybrid of quantum and classical computational resources.

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Hybrid developer environment

How do we make it easier for users to develop hybrid applications?

stay tuned for the Ocean Update Wednesday morning ...

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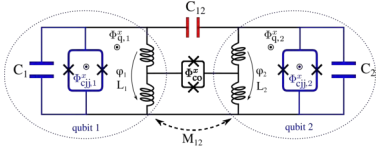
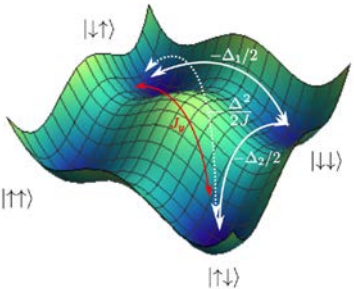
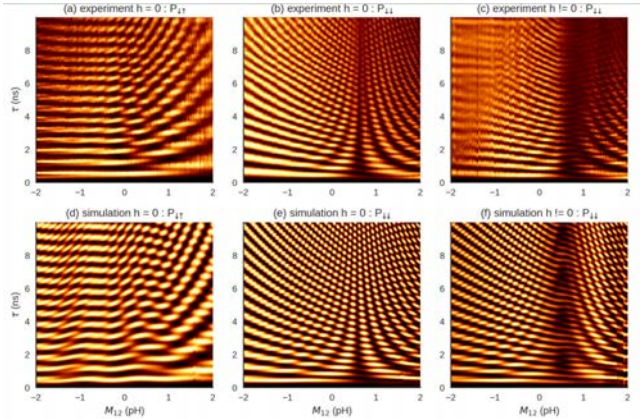
Towards universal computation

$$\mathcal{H}_S(s) = -\frac{1}{2}\sum_{i=1,2}\sigma_{x,i} - \sum_{i=1,2} h_i\sigma_{z,i} + J_{zz}\sigma_{z,1}\sigma_{z,2} + J_{yy}\sigma_{y,1}\sigma_{y,2} + J_{xx}\sigma_{x,1}\sigma_{x,2}$$







Ozfidan, *et al.*, "Demonstration of nonstoquastic Hamiltonian in coupled supercond. flux qubits", `arXiv:1903.06139v1`

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Summary

The Advantage platform will feature a

- A more powerful process with more and better connected qubits
- Lower noise qubits to find better solutions more quickly
- New operating software designed for hybrid applications

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