Next Generation Quantum Annealing System

Qubits North America
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The Next Generation quantum annealing system will have

- A more powerful processor
  - 5000 qubits - to solve larger problems
  - Increased connectivity - to make easier posing of complex problems
  - Lower noise technology
    - *more accurate problem specification*
    - *higher performance annealing*

- Improved operating software

- A hybrid developer environment
Quantum mechanics helps find the optimum
The goal of quantum annealing (QA): model the Hamiltonian

\[ \mathcal{H}_S(s) = -\frac{A(s)}{2} \sum_i \sigma_{x,i} + \frac{B(s)}{2} \left[ -\sum_i h_i \sigma_{z,i} + \sum_{i<j} J_{ij} \sigma_{z,i} \sigma_{z,j} \right] \]

Progression of processor scale over time

- D-Wave One
- D-Wave Two
- 2000Q
- Next Gen
D-Wave 2000Q quantum annealing processor

128,472 Josephson junctions
18,305 composite flux DACs
10,960 QFP shift register stages
Advantage™ qubits are more connected

### Specifications

<table>
<thead>
<tr>
<th></th>
<th>2000Q</th>
<th>Advantage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Qubits</td>
<td>2000</td>
<td>5000</td>
</tr>
<tr>
<td>Couplers</td>
<td>6000</td>
<td>40000</td>
</tr>
<tr>
<td>Josephson Junctions</td>
<td>128,000</td>
<td>1,030,000</td>
</tr>
<tr>
<td>Wiring</td>
<td>42 m</td>
<td>110 m</td>
</tr>
<tr>
<td>Active Area</td>
<td>$(5.5 \text{ mm})^2$</td>
<td>$(8.4 \text{ mm})^2$</td>
</tr>
<tr>
<td>On-chip memory</td>
<td>22 kiloByte</td>
<td>130 kiloByte</td>
</tr>
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</table>
A closer look ...

The new graph, and embeddings on it can be explored now in the Ocean tools: ocean.dwavesys.com
### Basic graph embedding statistics

<table>
<thead>
<tr>
<th>Graph Type</th>
<th>2000Q</th>
<th>Advantage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Complete Graph</td>
<td>64 (17)</td>
<td>180 (17)</td>
</tr>
<tr>
<td>Complete Bipartite</td>
<td>64x64 (16)</td>
<td>172x172 (15)</td>
</tr>
<tr>
<td>Cubic Lattice</td>
<td>8x8x8 (4)</td>
<td>15x15x12 (2)</td>
</tr>
<tr>
<td>Factoring Circuit</td>
<td>16-bit (16)</td>
<td>30-bit (15)</td>
</tr>
</tbody>
</table>

(max chain length)
Compare embedding of graphs with similar average degree

Chimera C16 - DW 2000Q

Pegasus P6 - 680 Qubit Prototype

<table>
<thead>
<tr>
<th></th>
<th>Chimera C16</th>
<th>Pegasus P6</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logical Qubits</td>
<td>366</td>
<td>318</td>
</tr>
<tr>
<td>Average chain length</td>
<td>5.6</td>
<td>2.1</td>
</tr>
<tr>
<td>Average degree</td>
<td>24</td>
<td>25</td>
</tr>
</tbody>
</table>
Why do we want to reduce device noise?

- Better control of problem and anneal specification
- Better performance of QA

“Quality” factor

\[ Q = \mathcal{A}(s)T_1(s) / \hbar \]
In pursuit of a lower noise technology

Regularly measure:

- low frequency flux noise
- 0th order Macroscopic Resonant Tunnelling (MRT) peak:
  (a measure of integrated high frequency $S_{\Phi}(\omega)$)

Ongoing program to reduce intrinsic noise:

- Test $\sim 250$ samples per year
- monitor process stability
- modify processes and materials
Quantum simulation

$$\mathcal{H}_{3D}(s) = -\frac{\Gamma(s)}{2} \sum_i \sigma_i^x + J(s) \sum_{\langle i,j \rangle} J_{ij} \sigma_i^z \sigma_j^z$$

topological phase transition

transverse field cubic Ising lattice
New operating software to provide better support for hybrid applications

We believe the first quantum application that will bring value to a customer will use a hybrid of quantum and classical computational resources.
Hybrid developer environment

How do we make it easier for users to develop hybrid applications?

stay tuned for the Ocean Update Wednesday morning ...
Towards universal computation

\[ \mathcal{H}_S(s) = -\frac{1}{2} \sum_{i=1,2} \sigma_{x,i} - \sum_{i=1,2} h_i \sigma_{z,i} + J_{zz} \sigma_{z,1} \sigma_{z,2} + J_{yy} \sigma_{y,1} \sigma_{y,2} + J_{xx} \sigma_{x,1} \sigma_{x,2} \]

The Advantage platform will feature a

- A more powerful process with more and better connected qubits
- Lower noise qubits to find better solutions more quickly
- New operating software designed for hybrid applications